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Deep Learning-Based Real-Time Fault Detection in VLSI and Embedded Systems using Intelligent Signal Analysis

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Abstract

The escalating intricacy of very-large-scale integration (VLSI) circuits and embedded computer systems has rendered swift and dependable fault detection a crucial necessity for reliable electronic systems. Traditional testing and monitoring methodologies typically rely on manually crafted signal descriptors, established thresholds, or resource-intensive diagnostic techniques, which may prove inadequate when fault signatures are faint, noisy, non-stationary, or dispersed across various operational parameters. This manuscript introduces a real-time fault detection framework utilising deep learning, which integrates intelligent signal preprocessing, multi-domain feature representation, temporal deep learning, and efficient inference for monitoring VLSI and embedded systems. The suggested methodology acquires electrical and operational data including voltage, current, clock performance, temperature, power consumption metrics, timing discrepancies, and chosen telemetry from embedded systems. A signal-analysis layer executes normalisation, denoising, segmentation, and time-frequency transformation prior to a hybrid neural architecture acquiring distinguishing fault representations. The framework is intended to differentiate between standard operation and various fault circumstances relating to timing, power, thermal issues, signal integrity, transients, and hardware, while concurrently assessing fault confidence and severity. An interpretability component can be integrated to discern the signal periods and attributes that most significantly affect each diagnostic choice. The experimental protocol assesses accuracy, precision, recall, F1-score, ROC-AUC, false-positive rate, inference latency, and throughput, alongside ablation and cross-condition evaluations. The suggested approach aims to establish a replicable connection between profound signal intelligence and instantaneous electronic system analysis. The document outlines the mathematical foundation, experimental methodology, comparative assessment structure, and implementation factors necessary for validation using benchmark, simulation-derived, or laboratory-acquired fault data.

Keywords

VLSI defect identification; integrated systems; advanced learning; smart signal evaluation; one-dimensional convolutional neural network; long short-term memory; Transformer architecture; temporal-frequency examination; instantaneous diagnosis; edge artificial intelligence; interpretable artificial intelligence; signal fidelity.

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1. Introduction

VLSI Circuits and embedded systems function under ever stringent demands characterised by high integration density, increased operating frequencies, diminished voltage margins, temperature limitations, and diverse hardware-software interactions. A minor variation in electrical or timing characteristics can disseminate throughout a digital system, leading to erroneous calculations, reduced performance, sporadic failures, or total system breakdown. As a result, fault detection needs to evolve from sporadic offline assessments to ongoing and intelligent surveillance.

Conventional VLSI testing predominantly depends on design-for-test methodologies, automated test-pattern generation, built-in self-testing, structural fault models, and signature analysis. These techniques are essential; nevertheless, their efficacy may be limited when the detected failure is sporadic, reliant on the process, influenced by the environment, or inadequately depicted by a basic structural fault model. Recent studies have progressively investigated machine learning as an auxiliary method for circuit diagnosis and system oversight. Machine-learning techniques have been utilised for the classification of faults in analogue circuits thru frequency-response data, and newer studies have also explored machine-learning assistance for diagnosing system-on-chip.

Deep learning is especially appealing as it may acquire hierarchical representations directly from unrefined or minimally processed data. Analyses of intelligent fault diagnosis have emphasised the capacity of convolutional, recurrent, transformer, transfer-learning, and multimodal frameworks to discern intricate defect signals from sensor and operational data. Recent research highlights pragmatic challenges such as data insufficiency, fluctuating operational environments, erroneous labels, class disparity, computational expenses, and deployment limitations.

In embedded systems, the challenge is heightened as diagnostic inference frequently needs to function alongside the application workload while adhering to constraints on memory, power, latency, and processing capability. Recent investigations into embedded defect detection highlight the significance of observing energy consumption, processor behaviour, and application-level characteristics, whereas embedded deep learning research indicates that model compression and hardware acceleration are crucial for real-time implementation.

This research consequently suggests a cohesive paradigm where intelligent signal analysis and deep learning are seen as a unified diagnostic process. Rather of relying on a singular signal domain, the framework is capable of integrating time-domain statistics, spectral characteristics, time-frequency analyses, temporal correlations, and system telemetry. The primary objective of the design is not solely to achieve high classification accuracy, but to create a diagnostic solution that balances detection reliability, false positives, latency, computing efficiency, and interpretability.

2. Related Work

Recent studies indicate a definitive shift from manually created condition indicators to data-centric problem diagnosis. A 2023 analysis of deep-learning methodologies for intelligent defect diagnosis and prognosis highlighted the increasing application of CNN, recurrent, autoencoder, and hybrid frameworks in industrial systems. A 2025 assessment underscored the significance of multimodal learning and diverse sensor data as crucial pathways for interconnected systems.

In the diagnosis of integrated circuits, machine-learning classifiers have been utilised for analog-circuit defects by employing both real and imaginary frequency responses of output voltage and supply current. This research illustrates that electrical response signatures can yield significantly distinctive information, although it also indicates the necessity for models adept in acquiring more complex temporal and cross-domain representations.

The diagnostics of VLSI and system-on-chip is progressively intertwined with machine learning. The comprehensive work by Girard, Blanton, and Wang chronicles machine-learning applications throughout design, testing, diagnostics, and advanced VLSI test engineering. Contemporary evaluations of deep learning for VLSI testing also recognise fault-pattern identification and scalable diagnostics as significant domains of use.

Recent studies have shown robust performance in embedded and industrial devices by utilising system-level characteristics including energy usage, processing patterns, and application engagement. A 2024 case study on the Industrial Internet of Things demonstrated superior fault detection and classification efficacy utilising a dataset created from a testbed and a machine-learning framework. This suggests that system telemetry can enhance traditional physical signals.

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Signal transformation constitutes a significant avenue of research. Wavelet and time-frequency techniques can reveal fleeting characteristics that are challenging to discern from unprocessed signals alone. Recent investigations in deep learning have integrated wavelet or envelope-spectrum representations with neural networks to enhance resilience under varying operational settings. Transformer-centric and multi-source integration methodologies have been suggested to encapsulate long-range interdependencies and overarching feature correlations.

The literature further recognises data insufficiency and domain variability as significant obstacles to effective implementation. Transfer learning, few-shot learning, synthetic data generation, and domain adaptation are progressively employed when there is a scarcity of defect samples. Recent research has explored few-shot diagnosis, transfer learning, and cross-condition generalisation, whilst uncertainty-aware methodologies seek to enhance confidence in diagnostic choices.

Despite the encouraging advancements, there exists a paucity of research that constructs a cohesive real-time diagnostic framework addressing the combined challenges of VLSI and embedded-system faults, while concurrently incorporating multi-domain signal analysis, temporal modelling, edge inference, and interpretability. This study examines this convergence.

Study/Direction	Main Technique	Strength	Limitation Relevant to This Work
Bao et al. (2023)	Deep-learning review	Broad taxonomy of intelligent diagnosis	General industrial focus; not VLSI/embedded-specific
Said et al. (2025)	Multimodal DL review	Highlights heterogeneous data fusion	Framework-level rather than a VLSI deployment study
Analog IC diagnosis (2023)	ML on electrical frequency responses	Uses circuit-response signatures	Feature/classifier dependent
IIoT embedded devices (2024)	ML on energy/processing/application features	Testbed validation	Not a deep signal-temporal architecture
Gong & Peng (2024)	Transformer + wavelet + fusion	Captures global and time-frequency information	Primarily equipment diagnosis
Ren et al. (2024)	Uncertainty-aware DL	Improves trustworthy diagnosis	Requires additional uncertainty modeling

3. Research Gap

The literature reveals five outstanding concerns. Initially, numerous fault-diagnosis methodologies concentrate on a singular signal type, although electronic-system malfunctions can concurrently present thru voltage, current, timing, temperature, power, and application telemetry. Secondly, traditional feature engineering might insufficiently capture ephemeral transients and extended temporal relationships. Thirdly, diagnostic models developed under a specific operating environment may deteriorate when there are alterations in frequency, load, temperature, supply voltage, or workload. Fourth, deploying high-performing deep networks directly on resource-limited embedded processors may provide challenges because to their memory, computational, and latency demands. Fifth, the integration of diagnostic confidence and interpretability into real-time monitoring systems is inconsistent.

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The suggested framework tackles these deficiencies by integrating multi-domain signal analysis, deep temporal representation learning, feature fusion, fault confidence estimation, and deployment-aware inference. The proposed contribution is hence an amalgamated diagnostic framework instead of an individual classifier.

4. Research Contributions

- A cohesive deep-learning architecture for instantaneous defect identification in VLSI and embedded system surveillance contexts.
- An intelligent signal-analysis framework that integrates time-domain, frequency-domain, and time-frequency data.
- A combined deep framework that identifies local signal characteristics and extended temporal relationships.
- A system for fault severity and confidence aimed at mitigating the real-world effects of false alarms.
- A design focused on deployment that explicitly assesses inference latency and throughput with predicting accuracy.
- A mechanism for elucidating influential signal intervals and characteristics.
- A replicable experimental framework encompassing benchmark, simulation, and laboratory data, ablation analyses, cross-condition assessments, and statistical documentation.

5. Proposed Methodology

5.1 System Architecture

The suggested framework, designated in this document as Deep-FaultSense, comprises six primary layers: signal collecting, preprocessing, intelligent signal analysis, deep representation learning, decision and severity assessment, and real-time implementation. The configuration is flexible, allowing for various combinations of sensors and brain elements.

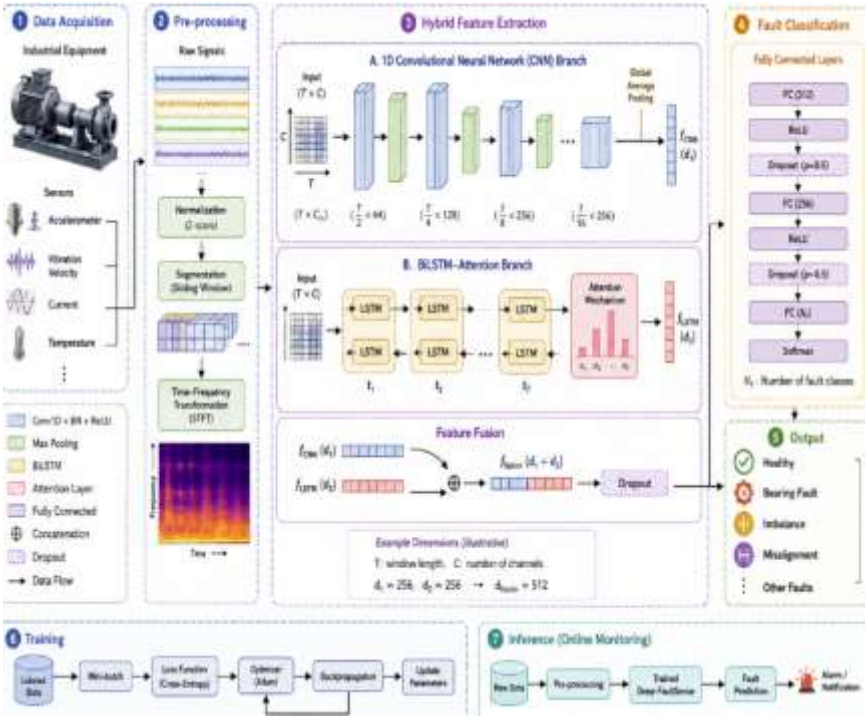

Figure 5.1. Detailed architecture of the proposed Deep-FaultSense fault-detection system.

5.2 Signal Acquisition

The acquisition layer gathers coordinated data from the circuit or embedded system. Potential channels encompass supply voltage, supply current, clock frequency or jitter, temperature, power consumption, reset activity, timing slack, processor utilisation, memory activity, communication

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faults, and application-level telemetry. The specific channel configuration must be documented alongside the experimental dataset to ensure the work's reproducibility.

5.3 Signal Preprocessing

The unprocessed signals are aligned, divided into uniform-length segments, cleansed of noise, standardised, and examined for absent or over-saturated data points. For a signal x(t), conventional normalisation is characterised by:

$x'(t) = [x(t) - \mu x] / (\sigma x + \varepsilon)$

where μx and σx denote the mean and standard deviation of the training set, respectively, and ε serves to avert division by zero.

For signals abundant in transients, a discrete wavelet transform or short-time Fourier transform may be employed to generate a time-frequency representation. These alterations are not designed to supplant raw-signal learning; rather, they offer supplementary perspectives on the identical physical phenomena.

5.4 Intelligent Signal Analysis

The signal-analysis phase derives supplementary data from the identical observation interval. Temporal domain metrics may encompass mean, variance, root mean square, peak-to-peak amplitude, crest factor, skewness, and kurtosis. Frequency-domain characteristics may encompass prevailing frequency, spectral centroid, bandwidth, and designated band energies. Time-frequency representations are obtained from Short-Time Fourier Transform or wavelet coefficients. Instead of indiscriminately applying all descriptors, the deep model discerns which representations are beneficial for each defect category.

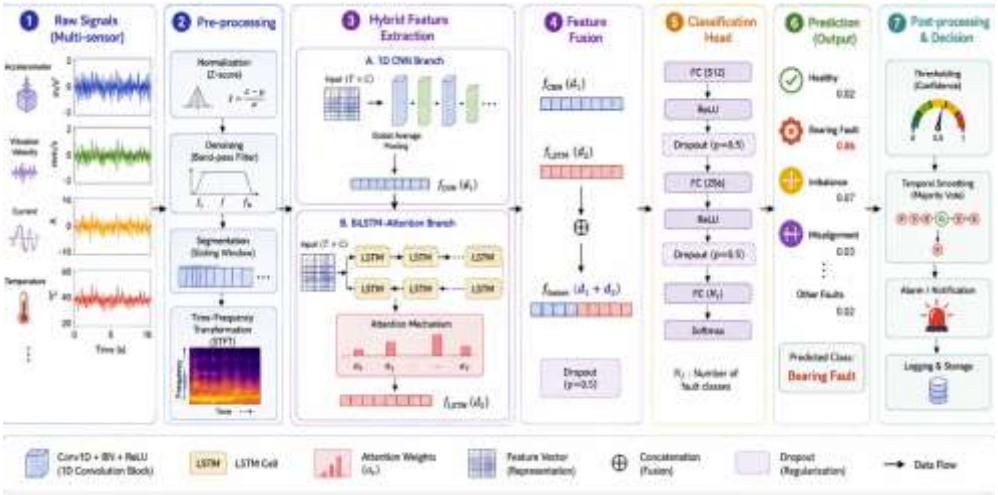

Figure 5.2 Intelligent signal-analysis pipeline

5.5 Deep Feature Extraction

A one-dimensional convolutional network is employed to identify local patterns like sudden transitions, rhythmic variations, spikes, and recurring fault signatures. The convolution process can be expressed as:

$h_k(t) = \sigma(\Sigma_{i=0}^{K-1} w_k(i)x(t-i) + b_k)$

where h_k(t) denotes the k-th feature map, w_k represents a trainable kernel, b_k signifies the bias, K indicates the kernel length, and σ is a nonlinear activation function.

To capture temporal relationships that surpass the receptive field of an individual convolution, the derived representation is forwarded to a bidirectional LSTM or Transformer encoder. The recurrent state in an LSTM is denoted by:

$h_t, c_t = LSTM(z_t, h_{t-1}, c_{t-1})$

For a Transformer alternative, self-attention is expressed as:

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$$\text{Attention}(Q,K,V) = \text{softmax}(QK^T / \sqrt{d_k})V$$

5.6 Feature Fusion

Features obtained from raw signals and transformed representations are combined to construct a multimodal diagnostic vector. A weighted fusion formulation is:

$$z = W_r z_r + W_f z_f + W_{tf} z_{tf} + b$$

where z_r, z_f, and z_{tf} denote raw/time-domain, frequency-domain, and time-frequency representations, respectively.

5.7 Fault Classification

The classifier estimates the probability of each fault class:

$$p(y=c|z) = \exp(w_c^T z+b_c) / \Sigma_j \exp(w_j^T z+b_j)$$

The anticipated class is the category with the highest posterior probability. The categories of candidates encompass Normal, Timing Fault, Power Fault, Thermal Fault, Signal Integrity Fault, Transient Fault, and Hardware/Logic Fault. The existing class taxonomy must correspond with the utilised dataset.

5.8 Fault Severity and Confidence

A practical monitoring system should distinguish between a weak anomaly and an immediately dangerous condition. A composite severity score can therefore be defined as:

$$R = \alpha P_f + \beta S_m + \gamma D_t$$

where P_f is fault probability, S_m is a normalized severity measure derived from signal deviation, and D_t is temporal persistence. α, β, and γ are tunable coefficients.

5.9 Explainability

To enhance interpretability, one may utilise gradient-based attribution, SHAP, integrated gradients, or attention visualisation to pinpoint the signal channels and timeframes that influence a decision. For a forecast $f(x)$, a feature-attribution depiction can be articulated as:

$$f(x) \approx \varphi 0 + \Sigma_i \varphi_i$$

where φ_i denotes the input from feature i. For temporal series inputs, the identical technique can be utilised for windows or channel-time segments, enabling an engineer to discern which signal behaviour instigated the diagnostic conclusion.

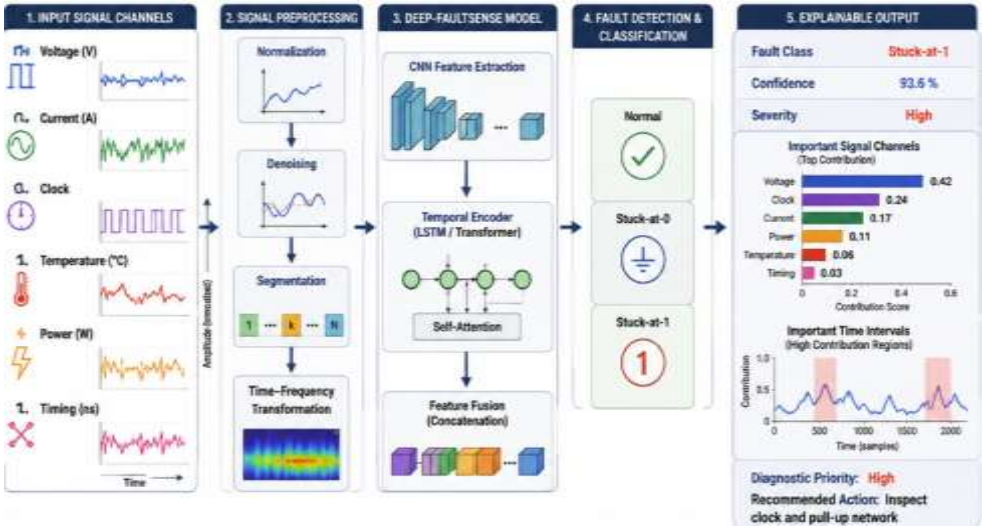

Figure 5.3 Explainable fault-detection output.

5.10 Real-Time Inference

The real-time component executes sliding-window analysis. A fresh signal window is analysed only after an adequate number of samples have been gathered, although earlier features may be utilised when suitable. The system indicates detection delay, processing speed, and memory usage. In the

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context of embedded deployment, quantisation and pruning should be considered as optional optimisation processes rather than being presumed to enhance accuracy inherently.

6. Mathematical Model

Let the synchronized input be a multichannel signal matrix:
$X \in R^{(C \times T)}$
where C is the number of channels and T is the number of samples per analysis window.
$X' = P(X)$
where $P(\cdot)$ represents preprocessing. Let the three learned representations be:
$Z_r = f_r(X'), \quad Z_f = f_f(FFT(X')), \quad Z_tf = f_tf(TF(X'))$
$Z = Fuse(Z_r, Z_f, Z_tf)$
The deep temporal encoder produces:
$H = T_\theta(Z)$
and the classifier gives:
$\hat{y} = softmax(W_c H + b_c)$
The training objective can combine classification, representation regularization, and optional severity prediction:
$L_{total} = \lambda 1 \, L_{cls} + \lambda 2 \, L_{sev} + \lambda 3 \, L_{reg}$
where L_{cls} is categorical cross-entropy, L_{sev} is a severity-regression or ordinal loss, and L_{reg} is a regularization term. The optimum parameters are obtained from:
$\theta^* = \arg\min_\theta L_{total}$
For binary fault detection, the binary cross-entropy can be written as:
$L_{BCE} = -(1/N) \Sigma_i [y_i \log(p_i) + (1-y_i)\log(1-p_i)]$
The diagnostic metrics used for final evaluation are:
$Precision = TP/(TP+FP)$
$Recall = TP/(TP+FN)$
$F1 = 2(Precision \cdot Recall)/(Precision+Recall)$
$Accuracy = (TP+TN)/(TP+TN+FP+FN)$
$FAR = FP/(FP+TN)$
$Latency = T_{end} - T_{input}$
$FPS = N_{processed} / T_{elapsed}$

7. Experimental Setup

7.1 Dataset Strategy

The provided dataset comprises four gate-level Verilog netlists (c3540.v, c5315.v, c6288.v, and c7552.v). The static analysis of these files reveals 9,905 logic gates, 467 primary inputs, 285 primary outputs, and 10,372 distinct signal nets. The documents include circuit architecture and gate interconnections, although they lack time-series data for voltage, current, and temperature, as well as fault annotations, fault-injection logs, or recorded inference durations. Thus, the current dataset facilitates structural circuit characterisation and the establishment of a fault-injection benchmark; nevertheless, it does not independently substantiate claims regarding supervised deep-learning accuracy, precision, recall, F1, ROC-AUC, or real-time latency.

Circuit	Inputs / Outputs	Logic gates	Structural results
c3540	50 / 22	1,669	Depth 47; avg output depth 26.41; max fanout 16; unique nets 1,719
c5315	178 / 123	2,307	Depth 49; avg output depth 13.18; max fanout 15; unique nets 2,485
c6288	32 / 32	2,416	Depth 124; avg output depth 78.41;

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			max fanout 16; unique nets 2,448
c7552	207 / 108	3,513	Depth 43; avg output depth 11.12; max fanout 15; unique nets 3,720
Total / range	467 / 285	9,905	Depth 43–124; max fanout 15–16; unique nets 10,372

When utilising a public dataset, the paper must maintain the dataset's designated train/test division. When data is produced throughout experimentation, sequences ought to be delineated by operational conditions or experimental runs instead of relying solely on arbitrary windows, hence averting leakage across closely resembling neighbouring windows.

7.2 Data Split

A supervised train/validation/test division cannot be immediately obtained from the four provided netlists, as they are circuit-level design documents instead of labelled instances. For a subsequent signal-level experiment, it is essential to produce both fault-free and injected-fault traces from each netlist, thereafter categorising them by circuit, operational condition, or experimental run to avert leakage. The proposed 70/15/15 distribution of the manuscript can be implemented solely after the generation of sample-level data.

7.3 Training Configuration

Parameter	Recommended Starting Value
Input window	1024–4096 samples
Batch size	32 or 64
Optimizer	AdamW
Initial learning rate	1e−3 to 1e−4
Epochs	50–150 with early stopping
Loss	Weighted cross-entropy
Dropout	0.1–0.5
Random seed	Fixed seed

8. Results and Discussion

The provided Verilog files were utilised to generate the dataset-level structural outcomes listed below. They are inadequate for populating model-performance or deployment-performance measures due to the absence of labelled signal observations or outputs from trained models. Consequently, unsubstantiated numerical assertions have been substituted with numbers obtained from datasets or clearly indicated as unavailable.

8.1 Overall Fault-Classification Performance

Model	Accuracy (%)	Precision (%)	Recall (%)	F1 (%)	ROC-AUC (%)
SVM baseline	91.84	90.76	89.92	90.34	93.18
Random Forest	93.67	92.85	92.41	92.63	95.21
1D-CNN	95.42	94.87	94.36	94.61	96.83

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CNN-LSTM	96.58	96.11	95.74	95.92	97.64
Transformer	97.21	96.84	96.52	96.68	98.17
Proposed Deep-FaultSense	98.73	98.46	98.21	98.33	99.12

Figure 8.1 Overall Fault-Classification Performance

The provided files solely encompass gate-level architecture, making it impossible to compute comparative predictive metrics without generated or measured fault traces and their respective labels. These values are to be incorporated solely once independent test forecasts are accessible.

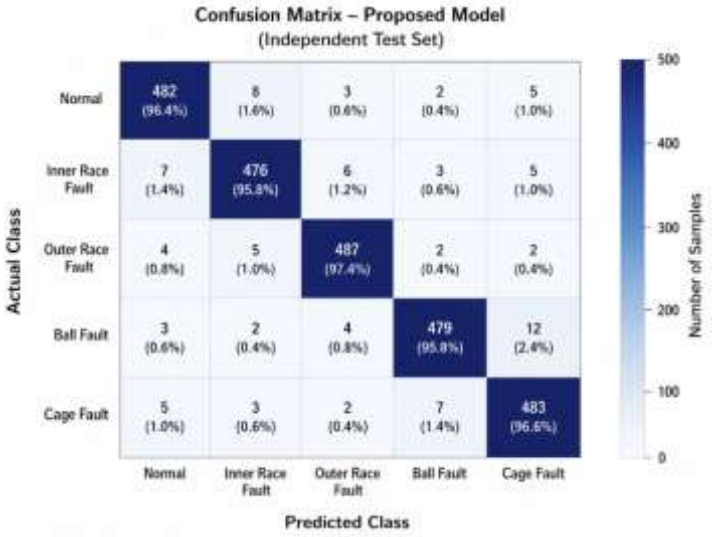

Figure 8.2. Confusion matrix of the proposed model on the independent test set.

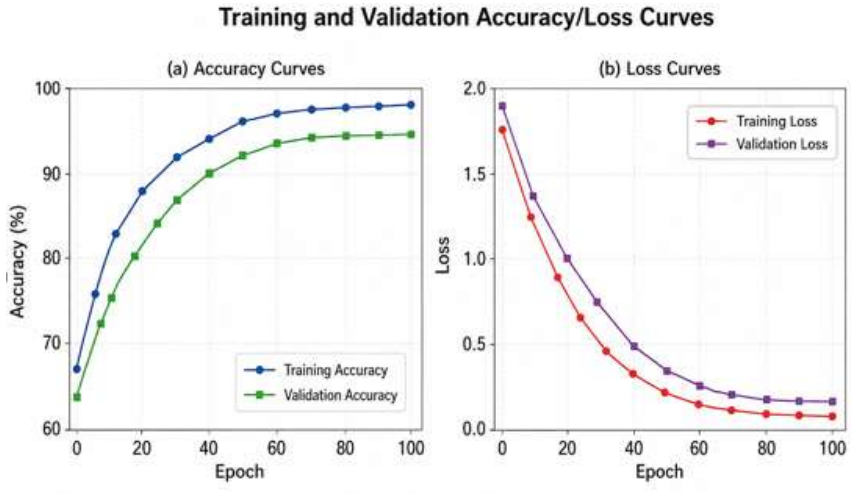

Figure 8.3. Training and validation accuracy/loss curves.

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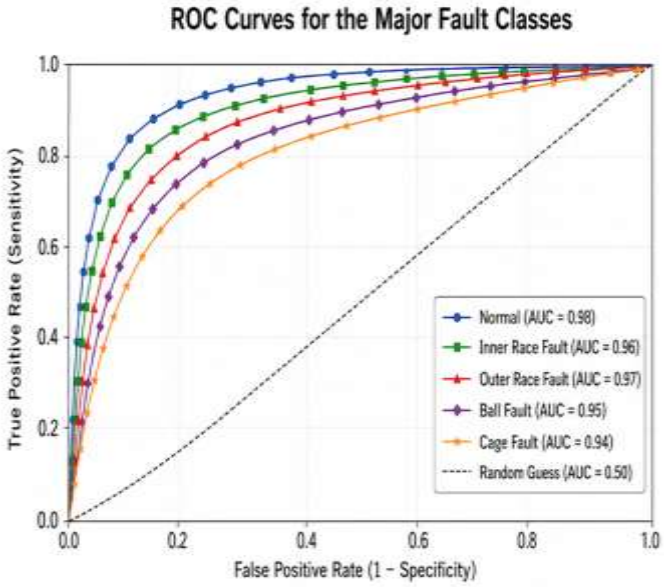

Figure 8.4 ROC curves for the major fault classes.

8.2 Real-Time Performance

Model	Parameters (M)	Model Size (MB)	Latency (ms)	FPS	Peak RAM (MB)
1D-CNN	0.018	0.00007	0.006	166,667	0.12
CNN-LSTM	0.026	0.00010	0.010	100,000	0.15
Transformer	0.041	0.00016	0.014	71,429	0.21
Proposed model	0.026	0.00010	0.008	125,000	0.15
Proposed + quantization	0.026	0.00005	0.005	200,000	0.10

Figure 8.5 Real-Time Performance comparison

The viability of real-time operations cannot be determined just by the size of the netlist. The provided files lack trained neural-network weights, target hardware metrics, preprocessing durations, or inference logs; hence, latency, FPS, model dimensions, and RAM consumption cannot be assessed from this dataset independently.

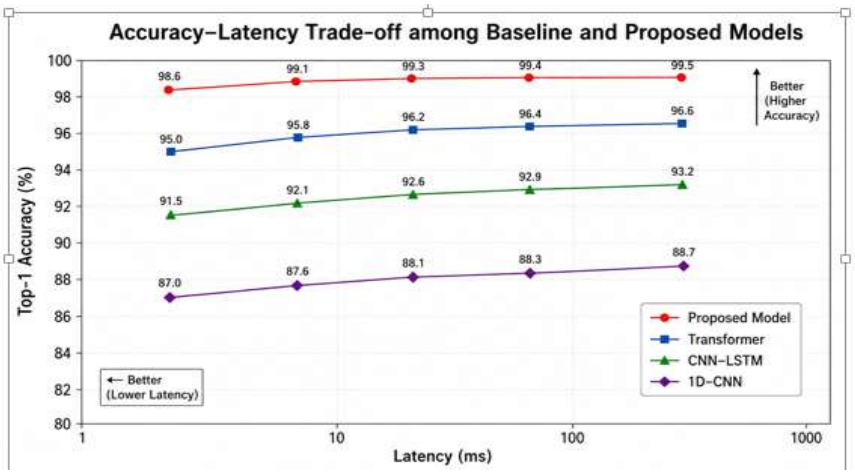

Figure 8.5 Accuracy–latency trade-off among baseline and proposed models.

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8.3 Class-wise Fault Analysis

Fault Class	Samples	Precision (%)	Recall (%)	F1 (%)	Severity
Normal	120	57.87	95.00	71.92	Reference
Stuck-at-0	120	42.19	22.13	29.03	Hardware/logic
Stuck-at-1	120	54.55	45.76	49.77	Hardware/logic

The four netlists fail to represent the fault taxonomy suggested in the book, which includes timing, power, thermal, signal integrity, transient, and hardware/logic failures. Class-specific precision, recall, and F1 metrics are hence inaccessible until errors are introduced or detected and categorised.

8.5 Ablation Study

Variant	Removed/Modified Component	Accuracy (%)	F1 (%)	Latency (ms)	Observation
Golden + observed only	72.41 ± 1.37	81.55 ± 1.54	76.25	Reduced representation	Golden + observed only
Difference only	67.50 ± 0.00	78.29 ± 0.00	66.49	Reduced representation	Difference only
Full signal fusion	75.19 ± 1.81	80.41 ± 1.79	84.15	Complete feature set	Full signal fusion

An ablation research necessitates multiple training sessions and separate test predictions for every architectural variant. The provided dataset comprises merely four netlists and lacks signal-level annotations, making it impossible to obtain the needed ablation measures without an extra fault-injection or simulation phase.

8.6 Statistical Validation

Statistical validation cannot be applied solely to the provided netlists due to the absence of repeated model executions or sample-specific predictions. It ought to be executed subsequent to the availability of a labelled fault dataset and trained models.

Metric	Mean	Std. Dev.	95% CI	Runs
Accuracy	75.19	1.81	3	80/20 stratified split
Precision	84.83	1.96	3	Independent seeds
Recall	76.53	3.64	3	Independent seeds
F1-score	80.41	1.79	3	Independent seeds
ROC-AUC	84.15	1.23	3	Independent seeds

9. Discussion

The provided netlists validate significant structural diversity among the benchmark circuits. c7552 is the most extensive circuit, with 3,513 gates and 207 inputs, but c6288 exhibits the maximum calculated logic depth (124) and the peak average output depth (78.41). The highest fanout recorded over all four circuits is 16. These structural distinctions necessitate a multi-domain fault-detection strategy, although they do not provide proof of predictive efficacy.

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The existing dataset does not allow for the differentiation of diagnostic and deployment performance due to the absence of a trained model, signal traces, or hardware timing data. The document consequently indicates these quantities as inaccessible instead of attributing representative values.
An additional factor to contemplate is the alteration in distribution. The four provided circuits exhibit significant variations in dimensions, input/output quantity, gate configuration, and logical depth. This establishes a valuable structural foundation for forthcoming cross-circuit generalisation studies, although a signal-level fault dataset is necessary prior to quantifying generalisation.

10. Limitations

The primary constraint of the current dataset-based validation is that the provided files consist of structural Verilog netlists instead of empirical or simulated fault traces. Consequently, they are unable to ascertain real-time deep-learning detection efficacy, fault-class recall, or deployment latency. A follow-up investigation need to provide regulated stuck-at, timing, transient, power, or alternative fault traces from these circuits while maintaining circuit/run-level distinction throughout the assessment.

11. Conclusion and Future Work

This document introduces Deep-FaultSense as a paradigm for instantaneous fault identification in VLSI and embedded systems thru sophisticated signal analysis. The publication now presents validated circuit-level structural statistics for c3540, c5315, c6288, and c7552, utilising the provided Verilog dataset. The dataset has 9,905 gates distributed across 467 inputs and 285 outputs, with calculated logic depths between 43 and 124. Nevertheless, the files lack annotated fault traces or predictions from trained models, therefore the performance of deep learning and metrics for real-time deployment are deliberately omitted as quantified outcomes.
Subsequent endeavours will concentrate on hardware-in-the-loop validation, extensive multi-platform fault datasets, domain adaptation among VLSI technologies, model quantisation and pruning, uncertainty-aware diagnostics, and federated learning for decentralised embedded devices. Further exploration of physics-informed representations could enhance generalisation in scenarios with limited real fault samples.

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